What is claimed is:

1. A semiconductor device comprising four chips each having on its surface a memory circuit and a plurality of pads including a plurality of address pads for use in inputting address signals of said memory circuit along with a plurality of input/output pads for inputting and outputting input/output data and also having a pair of long sides and a pair of short sides, a substrate supporting thereon said four chips and having on its surface a plurality of pads including address pads and input/output pads as electrically connected to respective ones of the address pads and input/output pads of said four chips, and a plurality of external terminals being electrically connected to the address pads and input/output pads on said substrate and including address terminals and input/output terminals as provided on a bottom surface of said substrate,

said four chips are disposed on said substrate in form of an array of rows and columns, the plurality of address pads of each of said four chips are disposed adjacent to one side of said pair of short sides, said plurality of input/output pads are disposed and spaced apart from one side of said pair of short sides toward the other side of said pair of

short sides when compared to said plurality of address pads, one of the pair of short sides of each of said four chips is disposed adjacent to one of the pair of short sides of its neighboring chip to permit the plurality of address pads of each of said four chips are placed at central part on a plane of said substrate, corresponding pads in the plurality of address pads of each of said four chips are commonly connected together to said address terminals of said external terminals, and the plurality of input/output pads of each of said four chips are connected to said input/output terminals of said external terminals independently of one another in units of respective chips.

2. The semiconductor device according to claim 1, said substrate is of a polygonal shape having a pair of long sides and a pair of short sides, said substrate has a multilayered wiring lead structure with electrical leads of a plurality of layers, said four chips are laid out into a matrix of two rows in a direction along the short sides of said substrate and two columns in a long side direction, address pads of chips laid out in the short side direction of said substrate are electrically connected together by a first lead layer extending in the short side direction

of said substrate, and address pads of chips laid out in the long side direction of said substrate are electrically connected together by a second lead layer being different from said first lead layer and extending in the long side direction of said substrate.

3. The semiconductor device according to claim 2, said first lead layer is an uppermost layer among the plurality of lead layers of said substrate, said second lead layer is a lowermost layer among the plurality of lead layers of said substrate, and said first lead layer and said second lead layer are electrically connected together by more than one through-hole filled with a conductive material as formed in said substrate.

4. The semiconductor device according to claim 3, said external terminals have lands used for connection of solder balls, said second lead layer is the same in level as the lands of said external terminals, and all of the lads of said external terminals are disposed on a bottom surface of said substrate in an area outside of said second lead layer.

5. The semiconductor device according to claim 4, said substrate is of a rectangular shape, said

address terminals of said external terminals are laid out at central part of a pair of long sides of said substrate of rectangular shape, and said input/output terminals of said external terminals are disposed at corner portions of said substrate.

6. The semiconductor device according to claim 5, more than one control pad for use in inputting a control signal of said memory circuit is further provided on each said chip, one of each pair of short sides of said four chips is disposed adjacent to a corresponding one of its neighboring chip to permit each control pad on each said chip to be placed on a center side on the plane of said substrate, each said control pad is commonized and connected to a control terminal of said external terminals, and said control terminal is disposed at central part of a long side of said substrate.

7. The semiconductor device as recited in claim 1, characterized in that the pads on each said chip are laid out into a linear array along a long side direction of each said chip at central part thereof.

8. The semiconductor device as recited in claim 1, characterized in that the pads on each said chip are laid out along the pair of long sides of each said chip.

9. The semiconductor device according to claim 1, the pads on each said chip are disposed along outside of the pair of long sides of each said chip.

10. The semiconductor device according to claim 1, each said chip is mounted on said substrate via a die-bonding material, the pads on each said chip are connected by bonding wires to the pads on said substrate, each said chip mounted on said substrate and said bonding wires are structurally arranged to be molded by a resin material, and said substrate is provided with a penetration hole for permitting escape of moisture vapor occurring due to thermal processing during solder reflow processes.

11. The semiconductor device according to claim 10, a step-like surface configuration correcting member made of a dielectric material is disposed at peripheral part of the penetration hole of said substrate.

12. The semiconductor device according to claim 10, said die-bonding material is prevented from being disposed at the periphery of the penetration hole of said substrate.

13. The semiconductor device according to claim 1, each said chip is mounted on said substrate by a face-down structure, and each said chip and said

substrate are coupled together by flip chip bonding techniques using metallic balls to have a structure with a resin material filled between a surface of each said chip and said substrate.

14. A semiconductor device comprising four chips each having on its surface a memory circuit and a plurality of pads including a plurality of address pads for use in inputting address signals of said memory circuit along with a plurality of input/output pads for inputting and outputting input/output data and also having a pair of long sides and a pair of short sides, a substrate supporting thereon said four chips and having on its surface a plurality of pads including address pads and input/output pads as electrically connected to respective ones of the address pads and input/output pads of said four chips, and a plurality of external terminals being electrically connected to the address pads and input/output pads on said substrate and including address terminals and input/output terminals as provided on a bottom surface of said substrate,

said four chips are disposed in a linear symmetrical fashion on said substrate in form of an array of rows and columns, the plurality of address pads of each of said four chips are disposed adjacent

to one side of said pair of short sides, said plurality of input/output pads are disposed and spaced apart from one side of said pair of short sides toward the other side of said pair of short sides when compared to said plurality of address pads, one of the pair of short sides of each of said four chips is disposed adjacent to one of the pair of short sides of its neighboring chip to permit the plurality of address pads of each of said four chips are placed at central part on a plane of said substrate, corresponding pads in the plurality of address pads of each of said four chips are commonly connected together to said address terminals of said external terminals, and the plurality of input/output pads of each of said four chips are connected to said input/output terminals of said external terminals independently of one another in units of respective chips.

15. A semiconductor device comprising four chips each having on its surface a memory circuit and a plurality of pads including a plurality of address pads for use in inputting address signals of said memory circuit along with a plurality of input/output pads for inputting and outputting input/output data and also having a pair of long sides and a pair of

short sides, a substrate supporting thereon said four chips and having on its surface a plurality of pads including address pads and input/output pads as electrically connected to respective ones of the address pads and input/output pads of said four chips, and a plurality of external terminals being electrically connected to the address pads and input/output pads on said substrate and including address terminals and input/output terminals as provided on a bottom surface of said substrate,

said four chips are each such that said input/output pads are of ×16 input/output bit configuration, corresponding pads in respective plurality of address pads of each of said four chips are connected in common to said address terminals of said external terminals, and the plurality of input/output pads of each of said four chips are connected to said input/output terminals of said external terminals in a way independent per each chip and are thus caused by said four chips to have ×64 input/output bit configuration.

16. The semiconductor device according to claim 15, said four chips each have an option-use pad with a bonding option function capable of permitting said input/output bit configuration to switch between ×16

and ×8, said substrate has an option-use pad with a bonding option function capable of letting said input/output bit configuration switch between ×16 and ×8, switching between the option-use pad on each said chip and the option-use pad on said substrate allows each of said four chips to exhibit either one of the ×16- and ×8-input/output bit configurations, and one of ×64- and ×32-input/output bit configurations is established by said four chips.

17. A semiconductor device including specified circuitry, a chip having on its surface a plurality of pads for use in inputting and outputting respective signals of said circuitry, and a substrate having on its surface a plurality of pads being electrically connected to the pads on said chip respectively, and a plurality of external terminals as electrically connected to the pads on said substrate respectively,

the pads on said chip and the pads on said substrate are structurally arranged so that they are connected together by bonding wires, first bonding is performed to the pads on said substrate, and second bonding is done to the pads on said chip.

18. The semiconductor device according to claim 17, metal balls are preformed at the pads on said chip, and said second bonding is applied to part

overlying said metal balls.